Available online at www.sciencedirect.com

SciVerse ScienceDirect

Procedia Engineering 47 (2012) 21 – 24

Procedia Engineering

www.elsevier.com/locate/procedia

Proc. Eurosensors XXVI, September 9-12, 2012, Kraków, Poland

Capacitance-controlled oscillator with enhanced tuning range using negative capacitance for time-based sensor interfaces

Jelle Van Rethy*, Georges Gielen

KU Leuven, Dept. Elektrotechniek ESAT-MICAS, Kasteelpark Arenberg 10, 3001 Heverlee, Belgium

Abstract

Since time-based sensor-to-digital conversion is gaining popularity in recent years, techniques to convert the sensor signal to a time-based signal are needed. Integration of a capacitive sensor in a capacitance-controlled oscillator (CCO) is one technique, but it suffers from sensor sensitivity degradation. To increase the sensitivity of the variation of the period of the CCO to the sensor variation, this paper proposes a technique which is based on cancelling part of the nominal capacitance C_0 of the sensor with a negative capacitance. To demonstrate the concept, the Signal-to-Noise Ratio is shown to increase with over 25% for a coupled sawtooth CCO, as is validated by simulations in UMC130 CMOS technology.

Keywords: Capacitive sensor; time-based conversion; capacitance-controlled oscillator; negative capacitance

1. Introduction

Time-based sensor interfacing benefits from the increased timing resolution in smaller CMOS technologies [1]. To process the sensor signal in the time domain, the sensor signal must first be converted to a time signal. One technique for capacitive sensors is to integrate the capacitive sensor directly into a ring oscillator where it functions as the capacitive load of one delay stage [1]. Capacitance-controlled oscillators (CCOs) thus offer direct conversion of a capacitive sensor to a time-based period signal, but a drawback of this technique is the limited Normalized Tuning Range ($NTR=\Delta T/T_0$). Based on the N-stage ring oscillator in Fig. 1 and formula (1), the NTR of the depicted ring oscillator, without the capacitance C_{comp}, is equal to $\Delta C/(N.C_0)$ if $C_{load}=C_0$.

* Corresponding author: Tel.: +3216321888; fax: +3216321975.
E-mail address: jelle.vanrethy@esat.kuleuven.be

doi:10.1016/j.proeng.2012.09.074

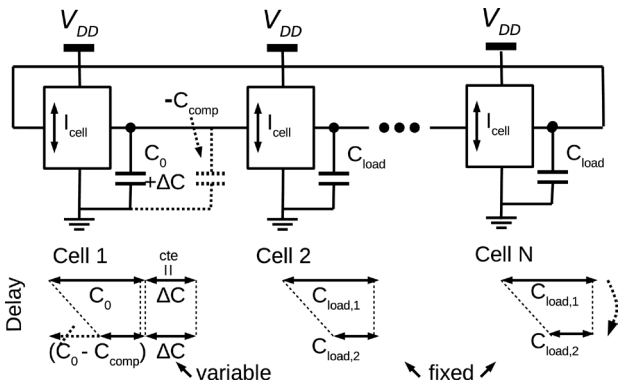


Fig. 1. Standard N-stage ring relaxation oscillator block scheme with integrated capacitive sensor in Cell 1. The delay as a function of the capacitive load per cell is indicated.

$$\left.\begin{aligned} T_0 &= 2\frac{C_0.V_S}{I_{cell}} + 2(N-1)\frac{C_{load}.V_S}{I_{cell}} \\ \Delta T &= 2\frac{\Delta C.V_S}{I_{cell}} \end{aligned}\right\} \Rightarrow \frac{\Delta T}{T_0} = \frac{\Delta C/C_0}{1+(N-1)\,C_{load}/C_0} \qquad (1)$$

This means that the original sensor sensitivity, which is equal to $\Delta C/C_0$, is already degraded by a factor N. To increase the NTR, ΔT should increase relatively to T_0. According to formula (1), this can be done by decreasing C_{load} (which is a fixed physical capacitance chosen by design), but this technique is limited by the parasitic capacitances or by the oscillator topology in order to guarantee the correct functionality [1].

This paper proposes a technique to increase the NTR by cancelling part of the sensor capacitance C_0 with a negative capacitance $-C_{comp}$ (see Fig. 1 dashed line). In this way, the total capacitance in the sensor stage that contributes to T_0 is (C_0-C_{comp}). The delay due to ΔC (ΔT) is now relatively larger compared to T_0. This is visualized in Fig. 1 and leads to a theoretical NTR of $\Delta C/(N.(C_0-C_{comp}))$ if $C_{load}=C_0-C_{comp}$. Since C_{load} can now be taken equal C_0-C_{comp}, the power consumption for the same free-running period T_0 will decrease [2]. However, less capacitive loading for the same period T_0 also leads to worse phase noise performance and thus to larger jitter σ_c on the time signal [2]. To combine both the NTR and the jitter σ_c in a single measure, the Signal-to-Noise Ratio (SNR) is calculated and is equated in formula (2).

$$SNR = 20.\log_{10}\left[\frac{NTR.T_0}{2\sqrt{2}.\sigma_c}\right] \qquad (2)$$

2. Negative capacitance generation

A negative capacitance can be generated via a capacitance in positive feedback over an amplifier (see Fig. 2 (a)) and is a technique that is already used to extend the bandwidth of amplifiers [3]. In Fig. 2 (a), the impedance Z_{in} seen on node n is equal to $[1/(s(C_0+\Delta C+(1-A)C_{comp}))]$. If gain A=2, the impedance is equal to $1/s(C_0+\Delta C-C_{comp})$. This means that an equivalent capacitance of $\Delta C+\mathbf{(C_0-C_{comp})}$ is seen at this node.

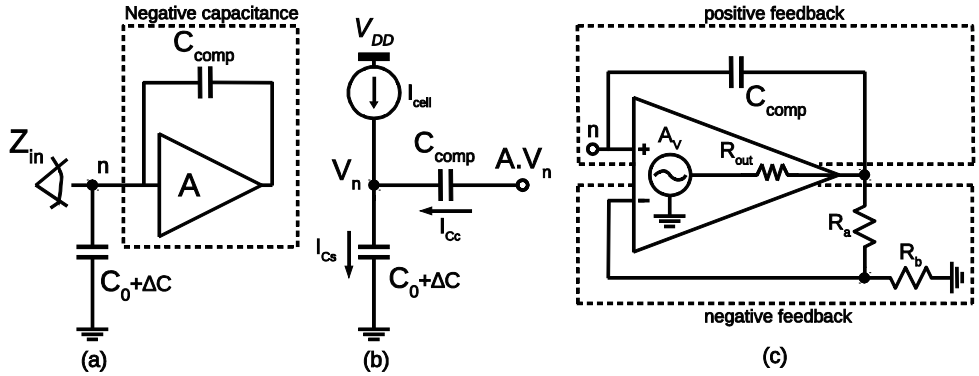


Fig. 2. (a) Block scheme of a negative capacitance C_{comp} generating network in parallel with C_0. (b) Equivalent network of (a) with the currents indicated. (c) Practical implementation of a negative capacitance circuit with an Opamp in negative and positive feedback.

In Fig. 2 (b), the currents which flow in the circuit are shown. In essence, the current through the compensation capacitance C_{comp} helps charging the large sensor capacitance C_0. One can calculate that the current I_{Cc} is equal to $I_{cell}.[(A-1).C_{comp}/(C_0+\Delta C - (A-1)C_{comp})]$ and thus is dependent on both I_{cell} and ΔC if the rest of the parameters are fixed.

A practical implementation with an ideal modeled opamp with gain A_V and output resistance R_{out} is given in Fig. 2 (c). In this setup we can locate both negative and positive feedback. Due to the negative feedback, the closed-loop gain is $A_V/(1+A_V.(R_b/(R_a+R_b)))$ and is approximately equal to $(R_a+R_b)/R_b$ if A_V is considered large. In this way we can also tune the negative capacitance seen at the input node with the resistors R_a and R_b according to the next equation: $Z_{in} = (-1/(sC_{comp}))*R_b/R_a$. This is very interesting, since we now have control on the amplitude of the negative capacitance.

3. Simulation results

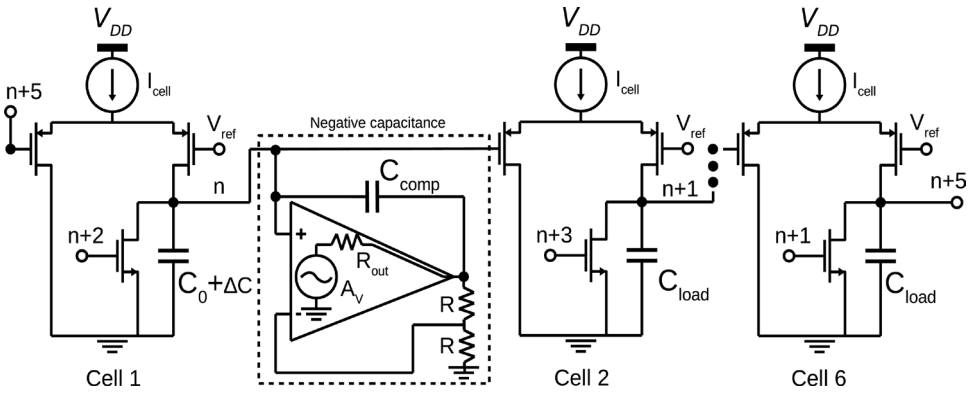
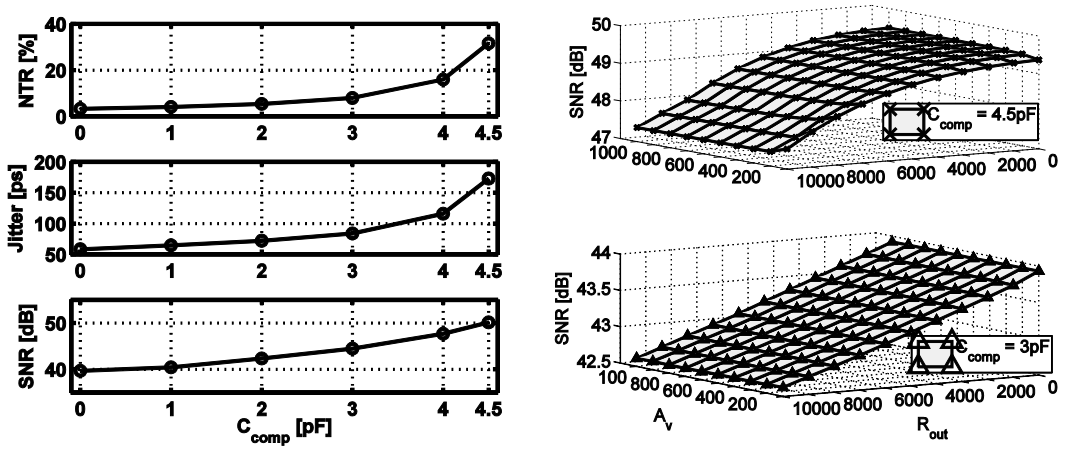


Fig. 3. 6-stage coupled sawtooth oscillator with a capacitive sensor integrated in Cell 1. In parallel with the sensor is a capacitance cancellation network with negative capacitance C_{comp} (R = 10k)

To validate the concept, simulations are done in UMC130 CMOS technology for a 6-stage coupled sawtooth CCO, as depicted in Fig. 3 [4]. In this oscillator design, the considered sensor has a nominal capacitance C_0 of 5pF and a variable range ΔC of 1 pF, which results in a sensor sensitivity of 20%.

The negative capacitance network is generated with an opamp with open-loop gain A_V and output resistance R_{out}. The closed-loop gain is taken equal to 2 in this setup by choosing both R_a and R_b equal to R, which is 10kΩ. This means that the negative capacitance seen at the input node of this network is $-C_{comp}$. Remark that the voltage swing of the oscillator itself is not equal to V_{DD} but is limited by V_{ref}. This is critical because the output swing of the opamp is twice the output swing of the oscillator (closed-loop gain is 2). This also means that this technique is not suited for every oscillator topology. However, the swing at the opamp's output can be reduced by decreasing the closed-loop gain and by increasing C_{comp} in order to obtain the same equivalent negative capacitance.

In Fig. 4 (a), both the NTR and the jitter σ_c are plotted as a function of C_{comp}. In order to make a fair comparison, the free-running period T_0 is equal to 500ns for each case. Although both the NTR and the jitter increase as a function of C_{comp}, the NTR increases more profoundly which results in an increase of the SNR as is clear from the bottom plot in Fig. 4 (a). In practical implementations, non-idealities in the opamp such as limited gain, limited output swing and non-zero output resistance will influence the SNR. Therefore the output swing of the opamp is limited to V_{DD} and both the gain A_V and output resistance R_{out} are swept. The resulting SNR is depicted in Fig. 4 (b) and from this plot it is clear that the influence of the non-idealities can be limited to a couple dB. For C_{comp} approaching 4.5pF, more than 10dB SNR, or an increase of 25%, can be obtained.



(a) (b)

Fig. 4. (a) NTR, jitter and SNR as a function of the compensation capacitance C_{comp} for T_0 = 500ns. (A_V = 1000 and R_{out} = 0). (b) SNR as a function of the gain A_V and the output resistance R_{out} of the opamp for C_{comp}=3 and 4.5 pF.

Acknowledgement

The first author is funded by FWO Vlaanderen.

References

[1] J. Van Rethy, H. Danneels, K. Coddens and G. Gielen, "Capacitance-controlled oscillator optimization for integrated capacitive sensors with time/frequency-based conversion" *in proc. of EUROSENSORS XXV,* September 2011

[2] A. Hajimiri, S. Limotyrakis, and T. Lee, "Jitter and phase noise in ring oscillators," IEEE JSSC, vol. 34, no. 6, pp. 790 – 804, 1999.

[3] A. Ghadiri, K. Moez ,"Gain-Enhanced Distributed Amplifier Using Negative Capacitance," *IEEE TCAS-I*, vol.57, pp. 2834-2843, 2010.

[4] Sander L. J. Gierkink and Ed (A. J. M.) van Tuijl, A coupled Sawtooth Oscillator Combining Low Jitter With High Control Linearity, *IEEE Journal of Solid-State Circuits*, Vol. 37, No. 6, June 2002.